Abstract

A novel, phase segregated bus differential protection scheme, which utilizes independent multi-principle advanced protection algorithms, such as, differential percent slope, delta phase directional comparison, rate of change of differential (ROCOD) currents, delta phase directional comparison on zero sequence current differential, fast CT saturation detection, second harmonic blocking and a check zone to secure the electrical bus bars upto three zones (two main and one transfer bus) will be discussed. Various combinations of the bus architectures or topologies can be protected with bus couplers, isolators, and CTs configurations including the end-faults detection capability.

The proposed advanced microprocessor based bus protection scheme does not require digital current inputs (sampled values) from Merging Units; instead, it has the ability to measure the conventional CT currents within the protection unit, and will share / distribute the sampled values using IEC 61850, 9-2 protocol, as a Merging Unit with other protection units to perform the overall differential protection. Each protection unit therefore acts as a processing (subscribing sampled values) and as well as a Merging Unit (publishing sampled values). The scheme can be scaled to support up to 24 bays (24 sets of three phase CT current inputs) and a three phase PT voltage input with 4 individual relay protection unit (6 sets of three phase CT current inputs per relay) functions together as one protection scheme, in a very compact electrical panel (4 x 3U rack units). For time synchronization, additional inputs, and outputs, an I/O unit is used to accommodate the breaker status, isolator status, and any other inputs into the bus protection scheme.

Keywords: Bus Differential Protection, sub-cycle, IEC 61850, Sampled Values, Process Bus (9-2), Station Bus (8-1), GOOSE, Merging Unit.
the elements connected to the bus. The requirement is to remove a faulted element from the power system by itself and not affect the remaining elements. If the fault is determined to be on the bus itself, it being a common component to all the connected elements, the correct required action would be to remove all elements connected to that bus in order to clear this fault from the power system.

The Bus Protection forms the vital part of the power system unit protection [1], where the reliability (dependability and security) is paramount as the entire substation power flow will be affected in case of miss operation of the protection scheme. There are many existing bus protection schemes available commercially to protect different bus configurations, but most of these schemes use either the proprietary protocols and/or complicated to understand and implement, and uneconomical.

The purpose of this paper is to present a multi-principle microprocessor based advanced bus protection scheme, which utilizes the international standard protocol (IEC 61850) for the exchange of sampled values (9-2) and the high speed GOOSE messages (8-1) to reflect the dynamic replica of the Isolator and Breaker status for monitoring different zones of bus protection. The proposed advanced microprocessor based bus protection scheme does not require current inputs from Merging Units; instead, it has the ability to measure the conventional CT currents within the protection unit, and will share/distribute the sampled values using IEC 61850, 9-2 protocol, as a Merging Unit with other protection units to perform the overall differential protection. Each protection unit therefore acts as a processing (subscribing sampled values) and as well as a Merging Unit (publishing sampled values). The scheme can be scaled to support up to 24 bays (24 sets of three phase CT current inputs) and a three phase PT voltage input with 4 individual relay protection unit (6 sets of three phase CT current inputs) functions together as one protection scheme, in a very compact electrical panel (4 x 3U rack units). For time synchronization, additional inputs, and outputs, an I/O unit is used to accommodate the breaker status, isolator status, and any other inputs into the bus protection scheme.

This advanced bus protection system measures currents from the conventional CTs and also publishes the IEC 61850 process bus based (9-2) protocol to exchange the sampled values amongst all the units using fiber optic/copper Ethernet communication. The IEC 61850 station bus (8-1) with high-speed GOOSE messages are also used to monitor the real time Isolator/Circuit Breaker status which allows for the dynamic reconfiguration of the CT inputs to different bus protection relay unit depending on the load – generation availability. The proposed bus protection scheme does not need any external Ethernet switch for the sampled value (9-2) exchange.

Very easy to use User Interface Windows software is used to set the Relay settings and for viewing Events, Fault logs, real time metering, and recording from any Relay unit. One logical recording will display all the channels (upto 24 bays), phase segregated differential protection quantities (operating and restraining) for further analysis. User definable logics further enhance customization capability with the available internal protection Relay logics.

Rigorous validation and testing has been performed using advanced RTDS (Real Time Digital System) and field captured COMTRADE file playback for switching, loading, inrush currents, extreme CT saturation conditions for external and internal faults. Many test cases for high impedance faults and faults on lightly loaded conditions have also been verified and will be discussed.

2. Multi-principles used for bus protection

For reliable operation of the bus protection scheme, multi-principles and supervisions are essential. This is especially true for the microprocessor based Relay system where the digital processing algorithms used to monitor the real time power system signals and the practical problems associated with the power system sensors such as CTs/PTs including the saturation of their iron core and distortion of the current signals during high speed Circuit Breaker operations needs independent principles to arrive at the reliable declaration of the internal/external or through faults.

The following multi-principles are used in the proposed architecture:

2.1 The slope miss match

This is the fundamental percentage differential scheme used in the percentage differential protection (Figure 1). Even though the miss-match of the operating and the restraining current gives the first indication of the type of fault, in many occasions, the miss-match does not conclude the final
operation (trip/block) of the relay with high reliability due to uncertainties associated with the practical measuring systems, including the primary CTs/PTs signals. Also, the percentage differential plane which uses the operating current, which is the magnitude of the vector sum of the currents from the same phase (A, or B, or C), and compares with the restraining current, which is the magnitude of the sum (algebraic sum) of the currents of the same phase (A, or B, or C) depends heavily on the magnitude of the currents and hence any miss-match due to the CTs, or magnitude / phase angle errors will allow the miss-match to trigger a trip, which is detrimental if only Slope miss-match principle is used. To increase the security aspect of the protection, the delta-phase directional technique is used as an independent principle as explained below.

![Percentage Differential Characteristic with Two Slopes](image)

**Figure 1 - The percentage differential characteristic with two slopes**

### 2.2 The delta-phase directional principle [2][3]

This principle essentially monitors the phase angle relationships with the incoming and the outgoing currents. With the microprocessor-based relays, implementing the phase angle in real time is a challenging task; hence a new (patent pending) dot product method is proposed which essentially suitable for the real-time implementations. The phase angles of the combination of various currents (incoming and out going) are executed in real-time using the dot-product method to compare whether the phase angle difference is within the threshold value to declare whether the fault is internal/or external to the zone of protection. In some situations, where the fault impedance is very high, and only one source is feeding the fault, the phase angle change may not be significant and hence this principle may take more time to declare the fault and hence this limitation has to be overcome with additional principles. The reference [4] uses similar technique wherein the phase angles of given phase current is compared with the differential or operating current. In the proposed approach, the phase angles of each phase currents are compared as explained below.

The delta-phase directional principle relies on the difference in phase angles between several current phasors. Calculating the phase angles, however, requires a relatively expensive “atan2(y,x)” standard mathematical library series expansion calculation even on an advanced microprocessor. Usually, the calculations should be carried out on 18 to 24 sets of inputs times the three phases, which would result in 54 or 72 inputs, and the combinations of comparing each input with others. Once the phase angle of the phasors has been calculated, then the difference between each pair of the 6 phasors (per phase) must be computed. This translates to 15 phase difference pairs per bus, for a total of 45 phase differences. The phase differences must further be normalized, since two phasors at angles of +10° and +350° respectively, are only 20° apart ... not 340°. This is a very challenging task to implement in real-time even on an advanced microprocessor.

#### 2.2.1 The vector dot product or delta-phase

Instead of computing each phasor’s phase angle, and then differencing pairs of phase angles (and subsequently normalizing the results), an indication of the difference in phase angles can be computed directly, using the dot product. For two vectors \( \mathbf{A} \) & \( \mathbf{B} \), the dot product is \( \mathbf{A} \cdot \mathbf{B} = |\mathbf{A}| |\mathbf{B}| \cos(\theta) \)
= A_x B_x + A_y B_y, where the term \(\cos(\theta)\) directly indicates the phase difference between the two vectors. The cosine of the phase difference, \(\cos(\theta)\), decreased as the phase difference, \(\theta\), increases. Specifically, for \(\theta<90^\circ\), \(\cos(\theta)\) is positive; for \(\theta>90^\circ\), \(\cos(\theta)\) is negative.

To determine if the phase difference, \(\theta\), between two vectors (shown in Figure 2) is greater than a specific set-point angle \(\theta_o\), we can instead test if \(\cos(\theta) < \cos(\theta_o)\), where \(\cos(\theta)\) is given by \(A \cdot B / (|A| |B|)\). Since \(\cos(\theta_o)\) is a constant, only evaluated once, no expensive transcendental functions are required after the relay has been initialized. Further, since \(|A|\) and \(|B|\) are both guaranteed to be positive, the inequality can be rewritten as: \(A \cdot B < |A| |B| \cos(\theta_o)\), eliminating the division operation.

![Figure 2 - The dot-product of two vectors A and B.](image)

### 2.2.2 Algorithm parameters

\(t_1\) = Amplitude below which the phase angles become erratic as the phasor magnitude approaches zero, any phasor with a magnitude less than this value (e.g. 0.1A) will be excluded from this algorithm. Furthermore, this value should be larger than the charging current for the line, in order to exclude lines where the breaker at the far end has been opened (e.g., \(I_{omn}\)).

\(\theta_o\) = Any phase angle differences greater than this value indicates there is no internal fault (90°). This phase angle limit is chosen, as the distortion due to the phase angle error due to saturation or any other physical phenomena will never exceed 90°.

### 2.2.3 Algorithm (executed per phase)

**Trivial reject**

- Examine magnitude of all current phasors.
- If no phasor is longer than threshold, \(t_1\), then there is no internal fault (Figure 3).

Find a phasor pair with a sufficiently large phase-difference

- For each pair, \(I_i \& I_j\), where \(i>j\), \(|I_i|>t_1\) and \(|I_j|>t_1\),
  - Compute \(I_i \cdot I_j\)
  - Compute \(|I_i||I_j|\ \cos(\theta_o)\)
  - If \(I_i \cdot I_j < |I_i||I_j| \cos(\theta_o)\), then there is no internal fault (Figure 4).
2.3 Rate of change of differential (ROCOD) [5]

This principle is essentially the extension of the principles of the Kirchoff’s current law, which can be stated as follows:

2.3.1 A review of existing concept:

The mathematical principle used in most low impedance differential protections used today to discriminate whether the fault is internal or external using Operating and Restraining currents as follows.

The operating current applied for a ‘n’ input bus protection device becomes:

\[ IO = |I_1 + I_2 + I_3 + \ldots + I_n| \]

The operating current is the phasor or vector sum of the currents entering and leaving the protection zone.

The restraining current is defined as:

\[ IR = |I_1| + |I_2| + |I_3| + \ldots + |I_n| / W \]
The restraining current is the sum of the absolute current magnitudes entering and leaving the protection zone. Typically, W has a value of 2.

The values and definitions of the operating and the restraining quantities are those generally used today for low impedance percentage differential relaying and has been in effect for at least the last 50 years of protective relay application starting with electromechanical relays.

In order to get a trip from the differential relay,

\[ \text{TRIP} \equiv IO > f(\text{IR}) \] \hspace{1cm} (3)

where \( f \) implies some function of IR, which is the “slope characteristics”.

The novel technique proposed by simply differentiating equation 3 (which is the same as differentiating equations 1 and 2) with respect to time on both the sides yields the ROCOD algorithm:

\[ \text{TRIP} \equiv \frac{d(IO)}{dt} > \frac{d(f(\text{IR}))}{dt} \] \hspace{1cm} (4)

The above ROCOD (Equation 4) algorithm is used to provide fault discrimination (internal or external to the protection zone) information, as depicted in the functional logic diagram (Figure 5). The derivative principle used in the ROCOD technique eliminates the constant load current effects on the restraining and operating currents of the protection zone. This is because the derivative of the constant, which is the load current as seen in Equation 4, will become zero. For all internal fault conditions, if \( \frac{d(IO)}{dt} > \frac{d(IR)}{dt} \), the fault will reside within the protection zone. Hence Equation 4 reflects the conditions for identifying internal faults reliably even under heavy load conditions or internal zone faults with high impedances.

The ROCOD logic is shown in Figure5.

a) The ROCOD logic is performed on a phase-by-phase basis.

b) The first top part of the logic checks to ensure that \( \frac{d(IO)}{dt} \) and \( \frac{d(IR)}{dt} \) are positive.

c) The next logic, checks to see if \( \frac{dIO}{dt} > \frac{dIR}{dt} \), as will be the case of a fault in the protected zone.

d) If conditions b & c are true, the fault will be deemed to be within the protection Zone

![Figure 5 - ROCOD logic for detecting the internal / external fault](image)

2.4 Zero sequence differential principle

For each set of input currents (A,B,C), the zero sequence differential of the operating current will be compared (shown in Figure 6) against the minimum operating current (set by the user). The zero
sequence differential will also be supervised by the delta-phase directional principle. This means the vector dot product of all the zero sequence differential currents of all the inputs at the bus are evaluated for the directionality as explained in section 2.2. This principle is also further supervised by the fast CT saturation detection, and the second harmonic restraint blocking.

![Diagram](image)

Figure 6 - The zero sequence directional principle using dot-product technique

The zero sequence differential is very sensitive to the earth faults, and with proper additional supervision, as stated above, this principle adds value to faster detection of the internal fault.

### 2.5 The check zone principle:

Protection of bus system with different zones utilizes the connectivity information from the Isolators and/or the Circuit Breakers from which the inputs (CTs) are measured. The zones of protection are carefully monitored for the generation and load balance at any time. During the transfer of load and/or generation from one zone to another, certain Isolators and/or Breakers are operated. During this event, if a fault occurs on the bus, the uncertain positions of the Isolators and/or Breaker positions may provide unexpected differential operating currents. It is very important to supervise the entire currents coming in and going out of the bus system irrespective of the Isolator and/or Breaker position at any time. The check zone principle will provide this supervision and hence it is very important in protecting bus systems with multiple zones with dynamic CTs configuration. The check zone utilizes independent percentage slope as explained in section 2.1.

### 2.6 Fast CT saturation detection:

When a bus fault happens with low fault impedance, the fault currents can reach very high values and may saturate CTs in their path. This is true for external as well as internal faults on any bus zone. The proposed method [6] accurately detects the fast CT saturation, and will provide proper blocking signal to the appropriate principles that are being supervised. The late CT saturation is taken care effectively by the principle explained in section 2.2. Typical early and late CT saturation responses calculated from the equivalent circuit are shown in Figure 7. There are also other techniques [7] available to detect the CT saturation based on the secondary current.
2.7 Second harmonic blocking:
The second harmonic contents in each phase of all the inputs are evaluated and the blocking is performed based on the second harmonic content (set by the user). The principles used in section 2.3 and 2.4 utilize this additional supervision.

3.0 Review of various bus system schemes or topologies:
There are a number of bus schemes or topologies used in practical power systems (shown in Figure 8, 9, 11 and 12), and the commissioning experience as described in [8]. Following is a review of various bus systems frequently used that can be protected using the proposed protection scheme.
3.1 End fault protection:

As shown in Figure 10, the end fault protection is required under the circumstances where the fault happens in the bind zone as shown inside the circle, between the circuit breaker and the CT and the bus CT is located on the line side.

If a fault happens between the circuit breaker and the CT as shown in Figure 10, and when the circuit breaker is in CLOSE position, then the bus protection system will trip respective bus zone depending on the Isolator status. Due to the nature of the topology, still the fault current will be flowing and hence a remote end circuit breaker trip command will be issued to clear the fault.

When the circuit breaker is in OPEN condition (Figure 10), if a fault happens between the circuit breaker and the CT, the bus zone protection will not issue a differential trip, since the relay will exclude this CT from the bus differential zone. In case where the main circuit breaker is in OPNE position and the transfer bus isolator is also in OPNE position, the relay will enable the end fault over current protection. This end fault over current information is used to enable the remote circuit breaker trip.

Figure 11 and 12 shows two typical bus configurations.
4.0 The IEC61850 architecture

The IED (Intelligent electronic device) is refereed below as bus protection relay unit, which can take upto 6 sets of three phase input currents as shown in Figure 13. The proposed bus protection scheme can be scaled to support upto 4 individual IEDs to protect upto 24 bays, with three independent zones. The following Figure 13 uses only two IEDs for illustrative purpose.

As mentioned in the previous sections, an additional I/O unit (Input / Output unit), which is also an advanced microprocessor device, is used which has dual role to play. The important function of this I/O unit is to provide a common time reference signal to all the bus protection IEDs in the form of 1PPS (pulse per second) to do synchronized sampling. The other important function of this I/O unit
is to provide Isolator/Circuit Breaker status with a capability up to 128 additional digital inputs and 16 output contacts. The time synchronization function will be explained in the later section in detail.

4.1 The network architecture for Sampled Value (9-2) and GOOSE (8-1) exchange

![Figure 14](image1.png)

Figure 14 - The network architecture for sampled value (9-2) and GOOSE (8-1) data exchange

In the above Figure 14, an illustrative two IED system with an I/O unit and its network connectivity is depicted. The Sampled Value exchange as per IEC 61850 (9-2) protocol can be accomplished using either fiber or copper Ethernet port, and additional external Ethernet switch is not essential. Similarly, the Isolator/Circuit Breaker status can be exchanged using high speed GOOSE messages as per IEC 61850, 8-1 over other Ethernet (fiber or copper) port available on the IEDs and the I/O unit. External Ethernet switch can also be used to accomplish the sampled value and GOOSE exchange.

4.2 The logical node used for sampled value exchange

![Figure 15](image2.png)

Figure 15 - The IEC 61850 logical node used for the sampled value exchange

As shown in Figure 15, the RMXU standard logical node as defined in IEC 61850, 7-4 ed 2 has been used for the sampled value exchange between different IEDs. In the proposed implementation, the sample rate used is 8 samples / cycle of the system frequency (50 or 60 Hz). The CT inputs are
sampled at much higher rate (96 samples /cycle), but for the differential protection, it is sufficient to have 8 samples / cycle. Therefore, there will be a down sampling done from 96 samples / cycle to 8 samples / cycle before the samples values are exchanged using the above logical node.

### 4.3 Exchange of sampled values through multicast control blocks

#### Table 9 – MMS TypeDescription definition for MSVCB MMS structure

<table>
<thead>
<tr>
<th>MMS component name</th>
<th>MMS TypeDescription</th>
<th>r/w</th>
<th>m/e</th>
<th>Condition</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>MsvCBNam</td>
<td>ObjecName</td>
<td>r</td>
<td>m</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MsvCRef</td>
<td>ObjecReference</td>
<td>r</td>
<td>m</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SVEna</td>
<td>Boolean</td>
<td>r/w</td>
<td>m</td>
<td>TRUE = transmission of sampled value buffer is activated. FALSE = transmission of sampled value buffer is deactivated.</td>
<td></td>
</tr>
<tr>
<td>MsvID</td>
<td>Visible-string</td>
<td>r</td>
<td>m</td>
<td>System wide unique identification.</td>
<td></td>
</tr>
<tr>
<td>DataRef</td>
<td>ObjecReference</td>
<td>r</td>
<td>m</td>
<td>MMS object name: the value of this component shall be of the format of ObjectReference and shall be limited to VMD or Domain scoped NameVariableList.</td>
<td></td>
</tr>
<tr>
<td>ConfRev</td>
<td>Integer</td>
<td>r</td>
<td>m</td>
<td>Count of configuration changes regarding MSVCB.</td>
<td></td>
</tr>
<tr>
<td>SimpRate</td>
<td>Integer</td>
<td>r</td>
<td>m</td>
<td>Amount of samples per period.</td>
<td></td>
</tr>
<tr>
<td>OptRef</td>
<td>refresh-time</td>
<td>Boolean</td>
<td></td>
<td>TRUE = 5V buffer contains the attribute “RefTm”. FALSE = attribute “RefTm” is not available in the 5V buffer.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>sample-synchronised</td>
<td>Boolean</td>
<td></td>
<td>TRUE = 5V buffer contains the attribute “SmpSynchron”. FALSE = attribute “SmpSynchron” is not available in the 5V buffer.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>sample-rate</td>
<td>Boolean</td>
<td></td>
<td>TRUE = 5V buffer contains the attribute “SmpRate”. FALSE = attribute “SmpRate” is not available in the 5V buffer.</td>
<td></td>
</tr>
</tbody>
</table>

Figure 16 - Multicast sampled value control block (MSVCB) and RMXU logical node usage

Once the logical nodes are designed, the sampled values of the phase currents (A,B, and C) is published by each of the IED to all other IEDs using a multi cast sampled value control block as shown in Figure 17. As indicated above, the sample rate and other mandatory items are appropriately filled in each multi cast sampled value block. In the proposed scheme, each IED can send up to 6 RMXU logical nodes per MSVCB, and an additional digital word (32 bits) for extra status information with the data set. Please refer to the diagram shown in Figure 17.

Figure 17 - The IEC 61850 services used with six CT input currents logical nodes in one physical bus protection device
4.4 The publisher and the subscriber architecture

Each IED has two services for the sampled value exchange. The SAV publisher will publish a MSVCB with 6 RMXU logical node information along with additional digital word in the data set. Totally, there will be 19 words of data that will be published using SAV publisher service from each IED.

On the subscriber service, the SAV Subscriber will receive up to 57 words of data (essentially from three IEDs each publishing 19 words). The sampled values are checked for the data integrity and the time alignment before it is passed onto the protection algorithm, which is executed 8 times in one cycle of system frequency (50 or 60 Hz).

In the event of late arrival of the sampled value packets (or missing data), bad data, miss alignment due to time synchronization, the protection algorithm will block the Relay operation and provide alarms for the appropriate events.

Once each IED (protection relay unit) receives the sampled values measured by rest of the other units, they all act as MASTER-MASTER relays, and all the relays respond (trip/block) simultaneously to the system event. This also adds redundancy into the bus protection scheme, and user can further enhance the logic by implementing the VOTING scheme or any other logics using enhanced user definable easy-to-use “PROLogics”. The tripping time for 5 times the nominal value magnitude of the fault current for 24 bays is less than 9 milliseconds, which assures the sub-cycle operations for 50 or 60 Hz system.

![Image](image18.png)

Figure 18 - The sampled value (SAV) subscriber and publisher architecture used in each bus protection IED

4.5 Time synchronization

A reliable time reference signal (which does not depend on the external time sources – such as GPS signal) is generated with an I/O unit to ensure the sampling synchronization and data alignment. External time sources such as IRIG-B, SNTP are also supported, if available, but are not essential for the differential protection. The simultaneous sampling time accuracy is +/- 5 micro seconds (around 0.1 degree). Various alarms will be generated for the unit synchronization / communication issues and appropriate blocking action will be performed instantaneously to secure the bus.

As shown in the Figure 19, the time synchronization starts with the I/O unit generating 1 PPS within the unit with reference to the free running real time clock (RTC). Later, this time is distributed to all the IEDs (protection units) to have common time reference using IRIG-B output from the I/O unit, which will be received by all the IEDs using their IRIG-B input. If the I/O unit receives any IRIG-B input from the external GPS clock or other resources such as SNTP, the same will be utilized to generate the IRIG-B output and will be distributed to the IEDs.

The time distribution will happen seamlessly whether external GPS clock is available or not and hence the protection system does not depend on any external GPS clock signal or time reference. This is important for the reliability of the protection.
5.0 The real time digital simulator (RTDS) results and discussions

A number of test cases have been simulated using the RTDS system and the real power system field COMTRADE signals for the proposed bus protection scheme. Following test cases are reported in this paper. All the tests are done on a 50 Hz system unless otherwise stated.

a) The 24 bays (24 sets of 3 phase currents) performance for 5 times the nominal pickup – Internal Fault.
b) Evolving external fault into internal bus fault.
c) High Impedance internal fault.
d) Extreme CT saturation during external fault.
e) Extreme CT saturation during internal fault.
f) Energization of transformer during internal fault.

5.1 The 24 bays performance for 5 times nominal the nominal pickup – internal fault

The RTDS simulation of 24 bays (24 sets of 3 phase currents from all the bays, shown in Figure 20) shows that the differential protection of Zone 1 on all the IEDs (up to 4 IEDs protecting 6 bays each) have operated as desired within 9 millisecond after the fault inception. This clear shows the response capability of the proposed bus scheme in terms of the sub-cycle operation even with fault current levels of only 5 times the nominal. As shown in the diagram, all the relays have taken decision simultaneously with no delay in their decision.
5.2 Evolving fault

This is the scenario where in, initially, the fault happens external to the bus zone, for example on the line and then after some time due to heavy fault current or close-in fault, the fault evolves as an internal fault into the bus zone. The Figure 21 shows the case of an evolving fault. As can be observed, the high miss match principle itself is not sufficient to secure the bus as the miss match (traditional percentage slope) has happened much earlier and would have miss operated the relay. But as stated in the earlier sections the proposed relay uses multi-principles to secure the bus and as desired the relay has operated correctly when the fault has evolved as an internal fault in the bus zone.

Figure 20 - The 24 Bay differential protection operation within 9 milli-seconds after the fault inception
5.3 High impedance fault

In many occasions, the fault current will have high impedance path, and hence it is very difficult to detect whether the internal fault has occurred. Usually the time of operation for such faults is relatively high due to the nature of the fault current, which is low due to the high fault impedance. The following simulation (shown in Figure 22) depicts this condition and the proposed relay has operated simultaneously on all the six bays within 24 milliseconds.

![Figure 22 - High Impedance fault with fault current 1.6A @ 5 deg, and a pickup level set to 1A](image)

Correct Operation of 87B Differential after the fault evolved into an internal fault

High Mismatch for external fault: not desired

Figure 21 - Evolving fault from external to internal bus zone
5.4 Extreme CT saturation with external fault

Following test case (shown in Figure 23) displays the bay 1 and bay 2 currents with extreme CT saturation. Due to the directional principle used (delta-phase), it can be seen that the bus protection scheme is very secured against the CT issues, and hence the protection scheme is in sensitive to the errors in the CTs and hence has low dependency on the accuracy of the CTs. Hence the relay secures the bus during external fault even with extremely distorted currents since it uses multi-principles, which are independent of each other.

![Figure 23 - Extreme CT saturation with external fault](image)

5.5 Extreme CT saturation with internal fault

![Figure 24 - Extreme CT saturation](image)
In the previous case with extreme CT saturation, the relay secured the bus for external fault. There are occasions in the bus faults that one or to CTs can saturate during the internal fault. The proposed relay is very selective as shown below (Figure 24). When an internal fault happens with similar extreme CT saturation, the relay operates within 13 milli-seconds and issues a trip signal.

5.6 Transformer energization during an internal fault

The following case shows the performance of the proposed relay during the energization of the transformer connected to the bus and during that time an internal fault occurs. Here again, the relay is very selective and tripped the bus due to the internal fault within 7 milli-seconds. Figure 25 shows the zone 1 trip, check zone trip along with the high miss match current.

![Image of Figure 25 - Transformer energization during an internal fault](image)

6.0 Conclusion

Advanced microprocessor based bus protection scheme, which utilizes the international industry standard IEC 61850 protocol for the sampled value (9-2) and high speed GOOSE (8-1) has been presented. The relay uses multi-principles to secure the bus against CT saturation, inrush currents, transformer energization, and other anomalies. At the same time, the proposed scheme reliably operates with security and dependability on the internal fault with extremely distorted currents from the CTs. The proposed scheme is scalable, flexible and very easy to use.

REFERENCES


